**ECE 3457**

**Lab 3: CMOS and Pseudo-nMOS Inverters**

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**Goal:**

Study CMOS and Pseudo-nMOS inverters.

**Task A:**

Measure and plot the iv characteristics of a CD4007 enhancement nMOS (one can use Lab1 results if using the same nMOS) and a pMOS transistor. For each, determine the threshold voltage, Vt, and the conductivity parameter, K. Use the measured K and Vt, run PSPICE or MultiSim and show simulated device iv.

**Task B:**

Design, build and simulate a CMOS inverter. Use VDD = 5 V. (1) Plot the load line and show intersections with the device iv curves. (2) Compute the VTC and plot results. (3) Measure the VTC and plot results. (4) Run PSPICE or MultiSim and show the simulated VTC.

**Task C:**

Repeat Task B for a pseudo-nMOS inverter.

**Theory:**

From Lab 1: (Task A)

The CD4007 enhancement nMOS and pMOS transistors have gate, drain, and source pins. The transistor has the equations

for when the transistor is operating in the triode region (VGS > VT and VDS ≤ VGS – VT) and

for when the transistor is operating in the saturation region (VGS > VT and VDS > VGS – VT). As the transistor enters the saturation region, the ID curve will begin to plateau. This is because the equation for current through the drain and source pins is not dependent on VDS when the transistor is operating in the saturation region. By obtaining the nMOS and pMOS transistors’ iv curves for different VGS values, it becomes possible to derive the value of K where

We can calculate the value of K and VT by plotting the square root of IDS against VGS according to the linear equation

Where the square root of K is the slope and VT is the x-intercept.

Lab 3: (Task B & C)

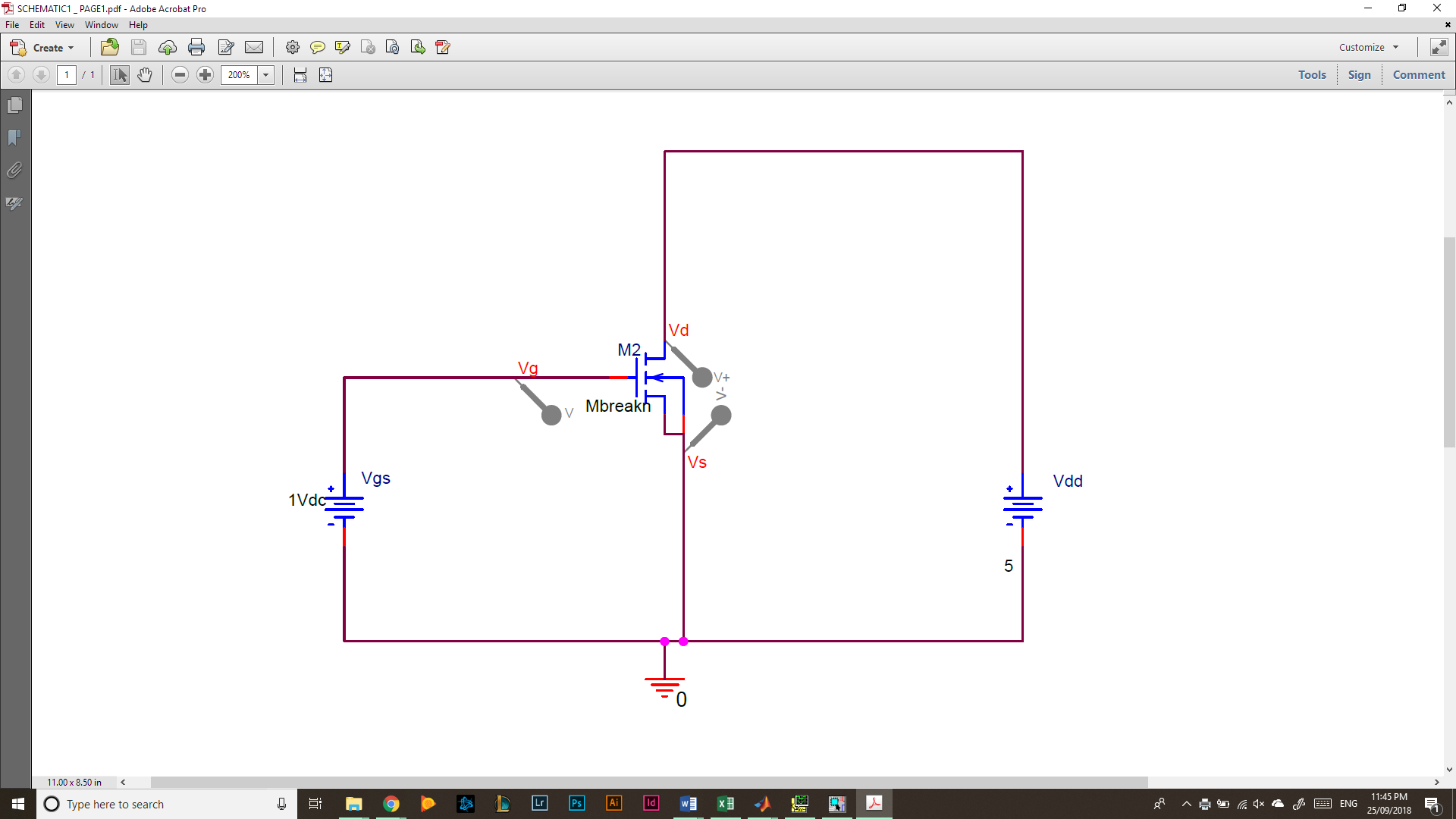
A transistor has 3 states: cutoff region, triode region, and saturation region. The transistor acts as an open circuit in the cutoff region, as such no current will flow. In the triode region, the current varies so the voltage across the transistor will also vary. When the transistor is operating in saturation mode, it’s current should no longer be changing dramatically so it acts like a small resistor, resulting in a small voltage reading across the transistor. Task B will have the transistors crossing multiple states, with different pairs for each section of the graph. i.e. QN Cutoff + QP Triode, QN Saturated + QP Triode, QN Saturated + QP Saturated, QN Triode + QP Saturated, and QN Triode + QP Cutoff. The circuit is Task C will not have as many transition states as the pMOS will always be on and operating in the saturation state for Vin < VTp and operating in the triode state for Vin > VTp. The nMOS will transition through cutoff, saturation, and triode states.

**Simulation & Experiment:**

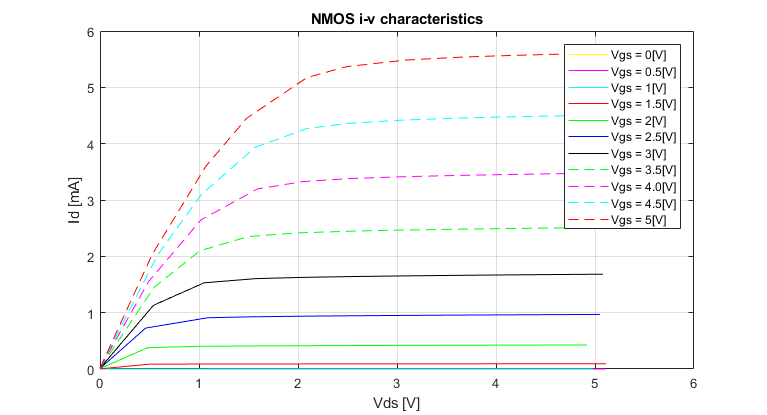
**Task A:**

**nMOS:**

The circuit was set up as below to test the iv characteristics of an enhancement nMOS.

  
*Figure 1: nMOS Test Circuit*

As in the above circuit, pin 3 was the gate voltage or VGS, pin 4 was the source voltage which was connected to ground, and pin 5 was the drain which was connected to VDS, or VDD according to Figure 1. Additionally, pin 7 (VSS) was connected to ground for proper operation of the chip. First VGS was set to 0 and then ID measured (the current through VD and VS) for VDD from 0[V] to 5[V] in 0.5[V] increments. Then VGS was incremented by 0.5[V] and the test for VDD and ID repeated. This process was repeated for VGS values from 0[V] to 5[V]. The following data was obtained for the nMOS transistor iv curves (tabular data at end of report).

  
*Figure 2: nMOS iv Characteristic Curves*

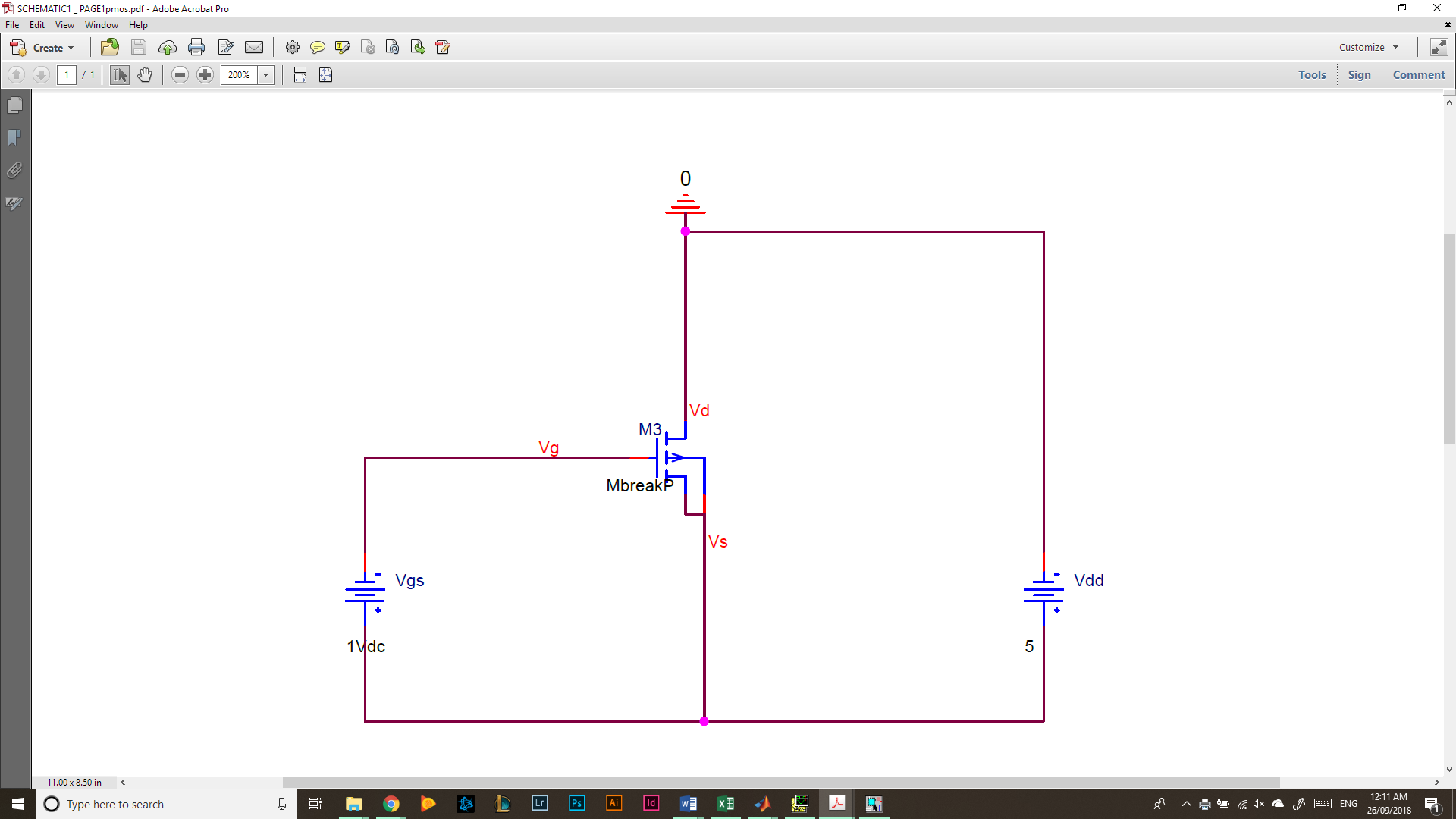
Values for K and VT can be found using this data. By selecting the current at which each transistor first enters saturation, or begins to plateau, a graph of the square root of ID vs VGS can be constructed. Currents that are consistently 0 across a VGS have been omitted.

*Figure 3: VGS vs ID1/2 For the nMOS Transistor*

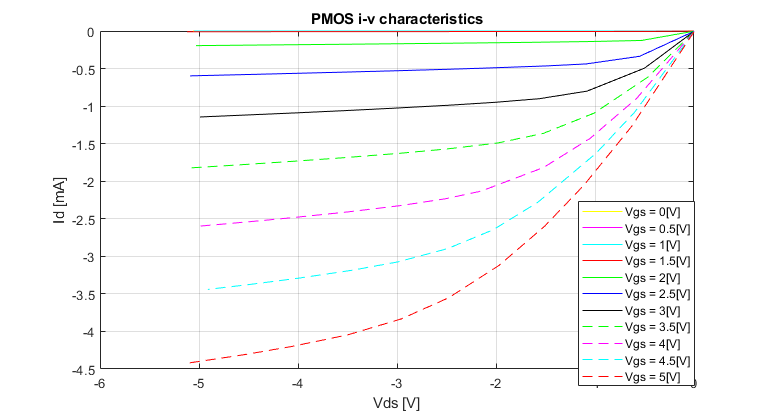
The slope of this line is 0.018515 which is equivalent to the square root of K. Therefore, the value of K is 342.8[μA/V2], the value of Kn is 685.6[μA/V2], and the value of VT is obtained by setting y to 0 and solving for x. Therefore, VT is equal to 0.91[V].

**pMOS:**

The circuit was set up as below for the pMOS circuit testing.

  
*Figure 3: pMOS Test Circuit*

Notice the voltage sources have been inverted from the previous test circuit. This was because the pMOS requires negative voltages for operation. Additionally, the ground was moved to the drain pin or pin 14 on the CD4007 chip. This was to ensure the chip functioned correctly as pin 14 was VDD and needed to be supplied the most positive voltage in the circuit to ensure proper operation. The source pin or pin 13 was connected to the positive terminals of VDD and VGS, and the gate pin or pin 3 was connected to the negative terminal of VGS. The voltages were set the same way as in testing for the nMOS and the following iv graph was obtained.

  
*Figure 4: pMOS iv Characteristic Curves*

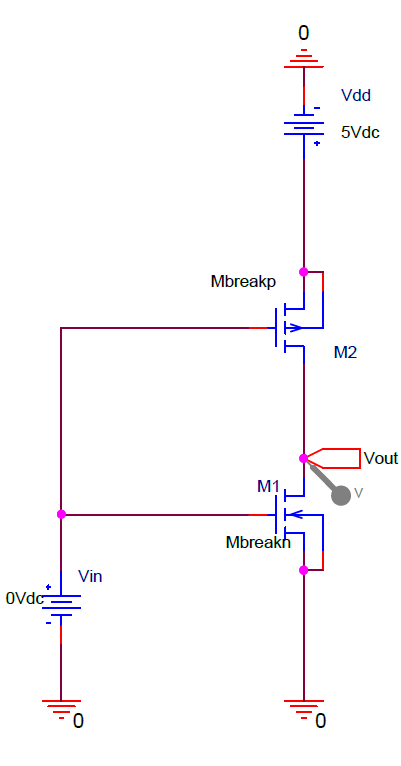
Values for K and VT can be found using this data. By selecting the current at which each transistor first enters saturation, or begins to plateau, a graph of the square root of ID vs VGS can be constructed. Currents that are consistently 0 across a VGS have been omitted.

*Figure 5: VGS vs ID1/2 For the pMOS Transistor*

The slope of this line is 0.017821 which is equivalent to the square root of K. Therefore, the value of K is 317.6[μA/V2], the value of Kp is 635.2[μA/V2], and the value of VT is obtained by setting y to 0 and solving for x. Therefore, VT is equal to 1.32 [V].

**Task B: CMOS Inverter Circuit:**

The circuit below was used for Task B involving a CMOS Inverter.

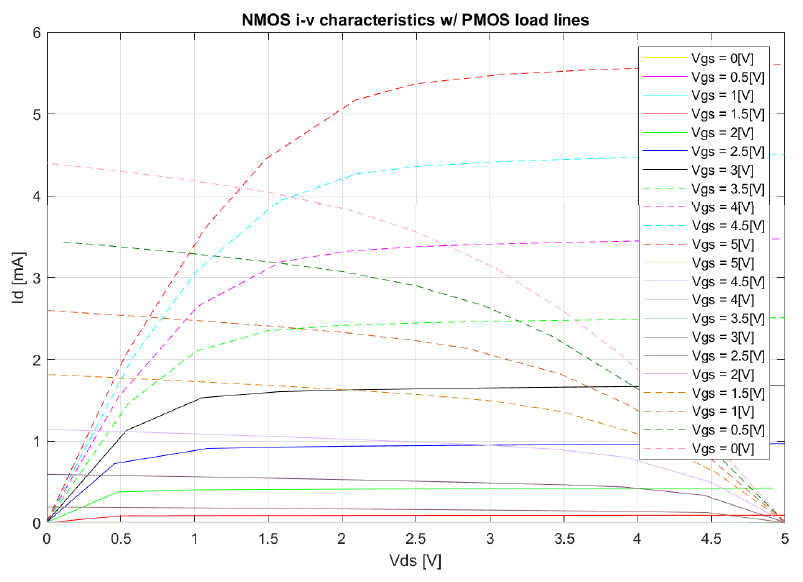


*Figure 6: CMOS Inverter Circuit*

VDD was set to a constant 5[V] and then Vin was incremented by 0.1[V] until it swept the voltage range from 0[V] to 5[V]. Vout was measured for each Vin value and the graph of Vin vs Vout was plotted to show the VTC.

1. **Graphical Analysis:**

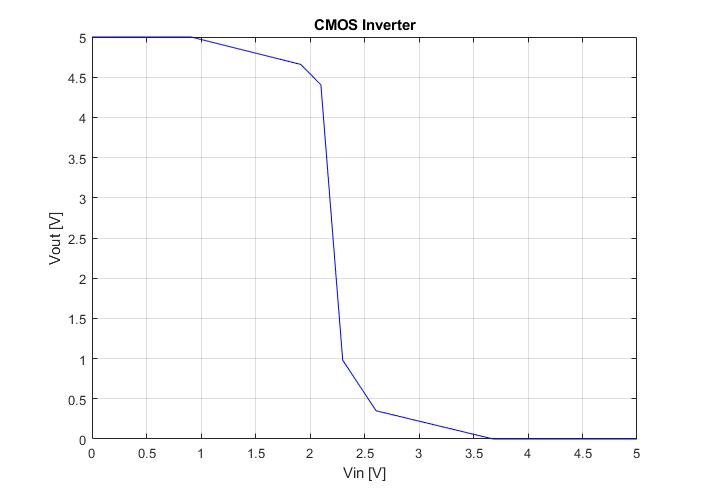
The load line can be calculated using the iv curves for the pMOS. The nMOS iv characteristics graph with load line is included below.



*Figure 7: nMOS iv Characteristics with Load Line for Task B*

1. **Computed VTC**

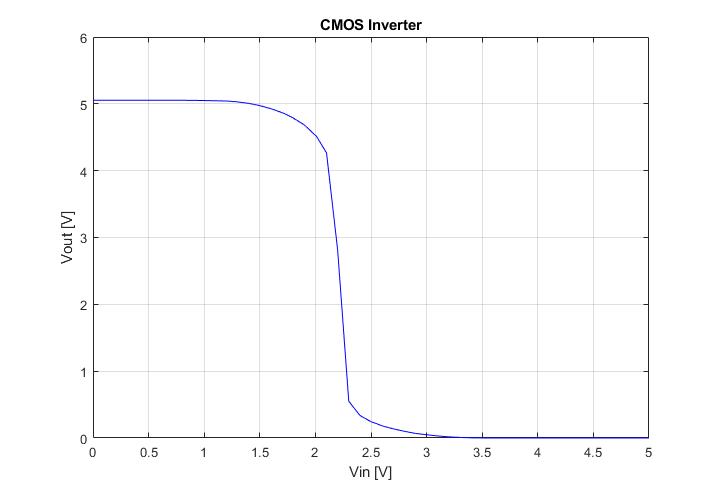
By calculating some critical points for the voltage curve of the CMOS inverter, we can create a rough diagram of the VTC. The below diagram used points at edges of the graph and transition points between transistor operating modes. This means the points were 5[V] output for 0[V] input and consequently 5[V] output for 0.91[V] input for the cutoff region of operation of the nMOS. The values 4.659[V] for output and 1.914[V] for input were calculated for the point where the VTC first has a slope of -1. The value of 2.269[V] was found for input where both transistors were in saturation. A value slightly less than this was used to determine a point just before the pMOS switched to the saturation region, i.e. Vin is 2.1[V] and Vout is 4.404[V]. A value slightly larger than this was used to determine a point just after the nMOS switched to the triode region, i.e. Vin is 2.3[V] and Vout is 0.980[V]. The values 0.351[V] for output and 2.607[V] for input were calculated for the point where the VTC has its next slope of -1. The last two points were when the pMOS entered its cutoff region and consequently Vout became 0[V] for Vin is 3.68[V] and 5[V].

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*Figure 8: Calculated CMOS Inverter VTC*

1. **Measured VTC**

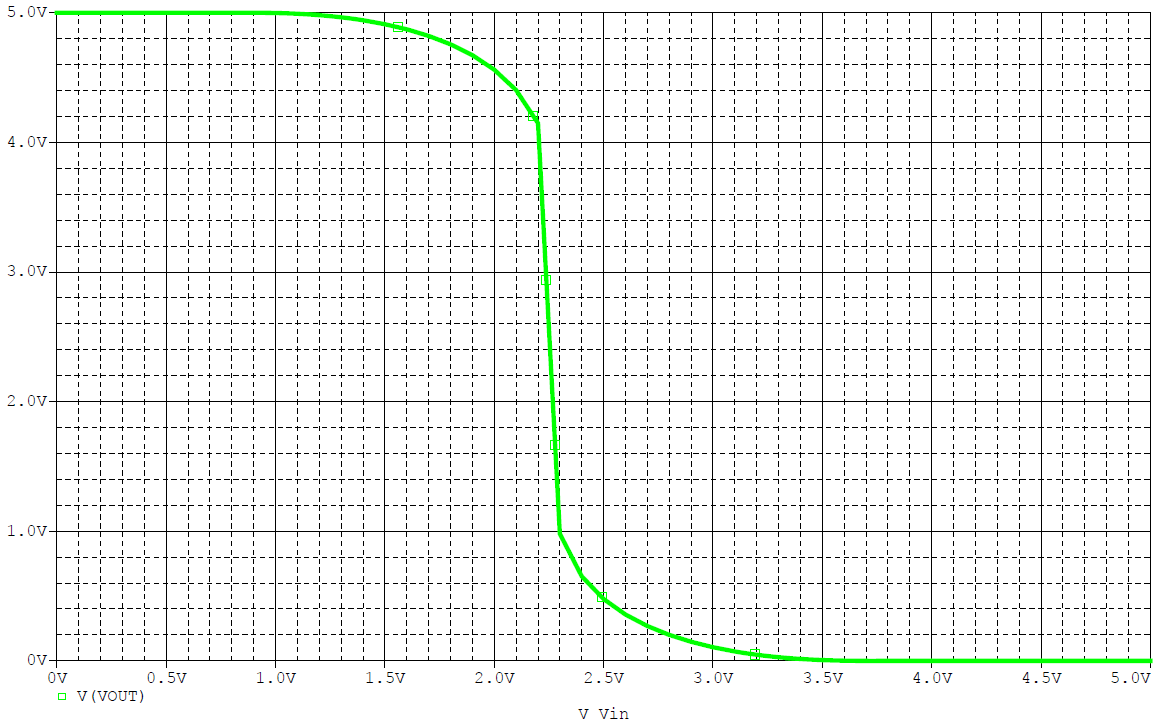
The data collected (see back pages) from the experiment set up according to Figure 6 is graphed below.

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*Figure 9: Measured CMOS Inverter VTC*

1. **Simulated VTC**

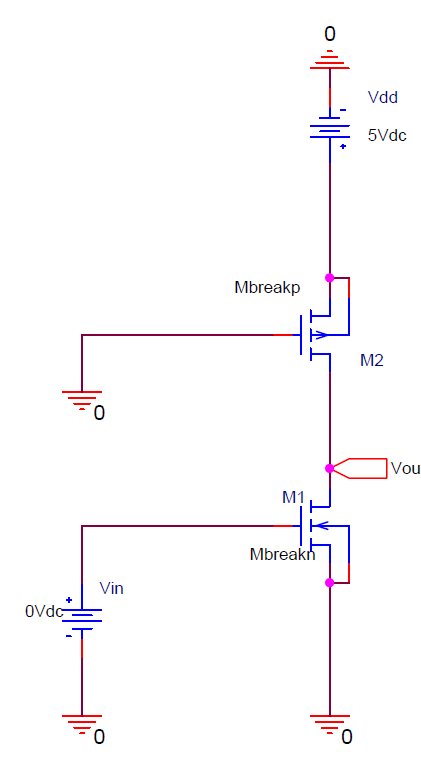
The circuit in Figure 6 was implemented in PSpice using VTn of 0.91[V] and Kn of 685.6[μA/V2], and VTp of 1.32[V] and Kp of 635.2[μA/V2]. The following VTC was obtained for this circuit.



*Figure 10: Simulated VTC for CMOS Inverter*

**Task C: Pseudo-nMOS Inverter**

The circuit below was used for Task C involving a pseudo-nMOS inverter.



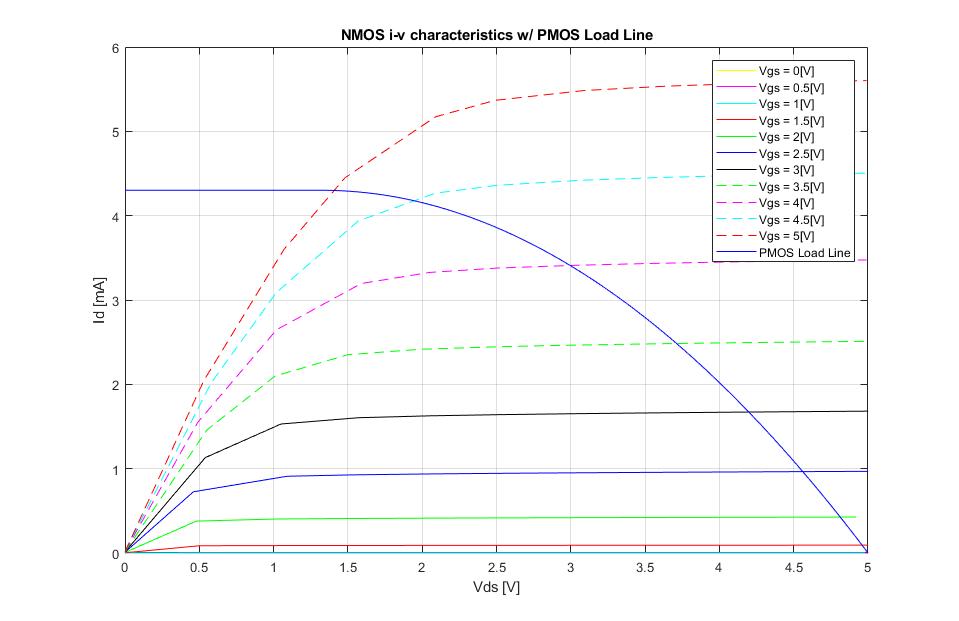
*Figure 11: Pseudo-nMOS Inverter Circuit*

VDD was set to a constant 5[V] and then Vin was incremented by 0.1[V] until it swept the voltage range from 0[V] to 5[V]. Vout was measured for each Vin value and the graph of Vin vs Vout was plotted to show the VTC.

1. **Graphical Analysis:**

The load line can be easily calculated as the pMOS is in the saturation region when VDS or Vout is less than 1.32[V] and operates in the triode region when greater than 1.32[V].

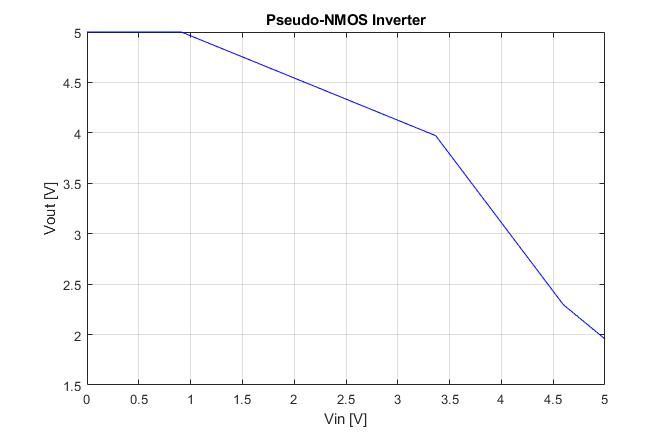
The nMOS iv characteristics graph with pMOS load line is included below.



*Figure 12: nMOS iv Characteristics with Load Line for Task C*

1. **Computed VTC**

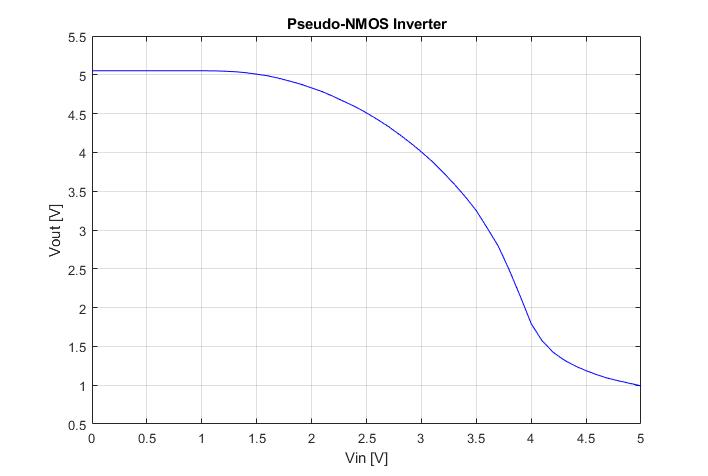
By calculating some critical points for the voltage curve of the pseudo-nMOS inverter, we can create a rough diagram of the VTC. This means the points were 5[V] output for 0[V] input and consequently 5[V] output for 0.91[V] input for the cutoff region of operation. The values 3.972[V] for output and 3.366[V] for input were calculated for the point where the VTC first has a slope of -1. The values 2.296[V] for output and 4.598[V] for input were calculated for the point where the VTC has its next slope of -1. The last point was calculated for when both the pMOS and nMOS were operating in their triode regions and Vout was calculated for Vin = 5[V]. Consequently, Vout was calculated to be 1.956[V].



*Figure 13: Calculated Pseudo-nMOS Inverter VTC*

1. **Measured VTC**

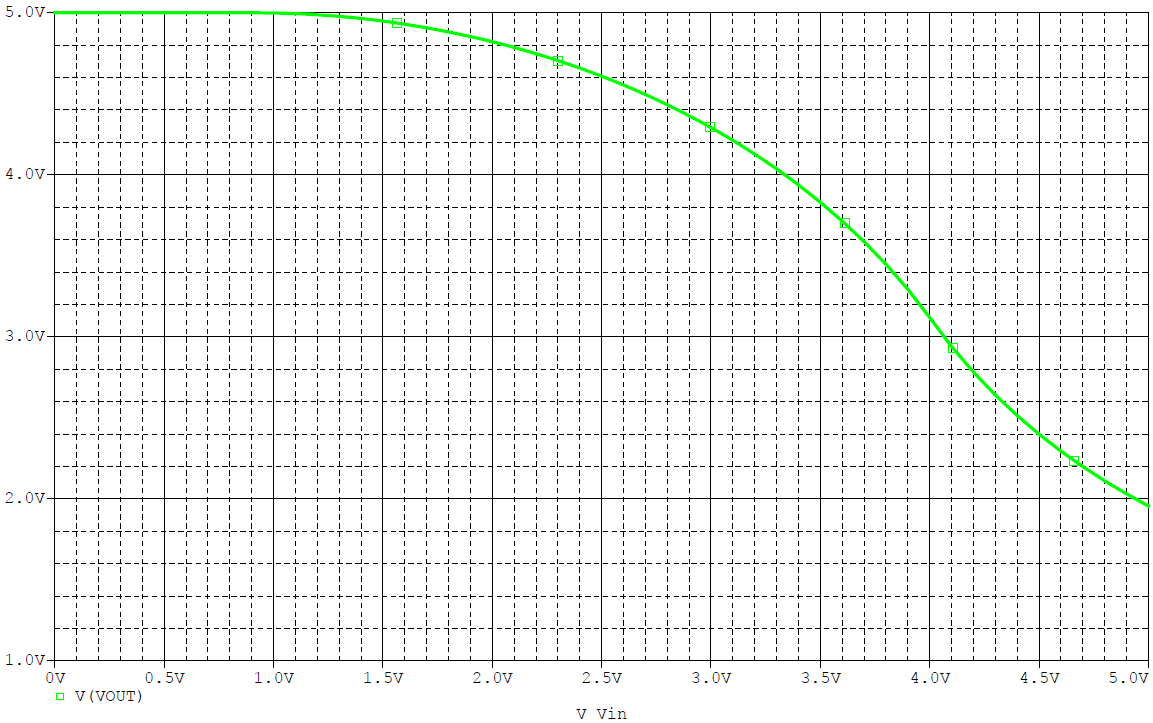
The data collected (see back pages) from the experiment set up according to Figure 11 is graphed below.



*Figure 14: Measured Pseudo-nMOS Inverter VTC*

1. **Simulated VTC**

The circuit was implemented in PSpice using the circuit in Figure 11 with a value VT of 0.91[V] and a Kn value of 685.6[μA/V2], and VTp of 1.32[V] and Kp of 635.2[μA/V2]. The following VTC was obtained for this circuit.



*Figure 15: Simulated VTC for Pseudo-nMOS Inverter*

**Analysis:**

The measured data matches the graphical analysis, calculated values, and simulation data in the case of the CMOS inverter from Task B. However, the measured data from Task C varies slightly from the values obtained from graphical analysis, computation of the VTC, and simulations of the circuit. While the circuit from Task B functioned according to expectations for all methods of analysis, Task C’s physical implementation did not behave as expected in theory. Task B’s behavior followed expectations with a cutoff region for Vin < VT and a VOH of ~5[V] across all testing. Lastly, all VTCs in Task B had a VOL of 0[V]. Task C differed in that all theory matched up to expectations, but the measured values for the circuit provided unexpected results. While the shape was similar for the first half of the Vin and Vout values, the VTC took a sharper slope towards the higher Vin values and ended with a Vout value 1[V] less than expected. The measured VOH of 5[V] was expected, yet the measured VOL of 1[V] at 5.0[V] Vin did not match the expected VOL of 2[V] at 5.0[V] Vin. The discrepancies are due to an incomplete understanding of the functionality of the CD4007 pMOS transistor chip.

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| vGS [V] | **nMOS** | **Tabulated** | **Data** |  |  |  |  |  |  |  |  |  |
| 0 | vDS [V] | 0 | 0.51 | 1.09 | 1.59 | 2.08 | 2.48 | 2.96 | 3.49 | 4 | 4.55 | 5.03 |
|  | iD [mA] | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0.5 | vDS (V) | 0 | 0.5 | 1 | 1.48 | 2.03 | 2.56 | 2.99 | 3.44 | 4.04 | 4.52 | 5.11 |
|  | iD (mA) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| 1 | vDS (V) | 0 | 0.49 | 1.09 | 1.64 | 2.01 | 2.64 | 3.1 | 3.56 | 4.02 | 4.51 | 4.98 |
|  | iD (mA) | 0 | 0.001 | 0.0011 | 0.0011 | 0.0011 | 0.0011 | 0.0011 | 0.0011 | 0.0011 | 0.0011 | 0.0011 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| 1.5 | vDS (V) | 0 | 0.5 | 1.03 | 1.47 | 1.98 | 2.47 | 3.1 | 3.65 | 4.05 | 4.54 | 5.11 |
|  | iD (mA) | 0.0026 | 0.0861 | 0.0882 | 0.0891 | 0.0898 | 0.0906 | 0.0913 | 0.0919 | 0.0923 | 0.0927 | 0.0932 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| 2 | vDS (V) | 0 | 0.48 | 1.02 | 1.58 | 2.07 | 2.48 | 3.07 | 3.63 | 4.09 | 4.53 | 4.92 |
|  | iD (mA) | 0.0066 | 0.3781 | 0.4031 | 0.4095 | 0.4133 | 0.416 | 0.419 | 0.4216 | 0.4235 | 0.4251 | 0.4265 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| 2.5 | vDS (V) | 0 | 0.46 | 1.09 | 1.53 | 2.09 | 2.59 | 3.09 | 3.58 | 4.06 | 4.55 | 5.05 |
|  | iD (mA) | 0.0094 | 0.7257 | 0.91 | 0.9265 | 0.9383 | 0.9456 | 0.9515 | 0.9564 | 0.9607 | 0.9649 | 0.9687 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| 3 | vDS (V) | 0 | 0.54 | 1.05 | 1.57 | 2.05 | 2.51 | 3.05 | 3.48 | 4.03 | 4.47 | 5.08 |
|  | iD (mA) | 0.0123 | 1.1308 | 1.5297 | 1.604 | 1.6266 | 1.6402 | 1.6523 | 1.6602 | 1.669 | 1.6751 | 1.6829 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| 3.5 | vDS (V) | 0 | 0.55 | 1.01 | 1.5 | 1.99 | 2.58 | 3.01 | 3.58 | 4.03 | 4.57 | 5.01 |
|  | iD (mA) | 0.0142 | 1.457 | 2.0986 | 2.3515 | 2.416 | 2.449 | 2.4648 | 2.4808 | 2.4915 | 2.5022 | 2.5101 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| 4 | vDS (V) | 0 | 0.49 | 1.02 | 1.59 | 2.05 | 2.51 | 3.03 | 3.51 | 4.04 | 4.52 | 4.99 |
|  | iD (mA) | 0.0165 | 1.5504 | 2.6471 | 3.1959 | 3.3268 | 3.3792 | 3.4115 | 3.4322 | 3.4504 | 3.4637 | 3.4752 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| 4.5 | vDS (V) | 0 | 0.58 | 1.02 | 1.57 | 2.09 | 2.51 | 3.06 | 3.58 | 4.06 | 4.49 | 5.13 |
|  | iD (mA) | 0.0181 | 2.0178 | 3.0908 | 3.9378 | 4.2673 | 4.361 | 4.419 | 4.4515 | 4.4735 | 4.4884 | 4.5085 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| 5 | vDS (V) | 0 | 0.53 | 1.07 | 1.48 | 2.09 | 2.49 | 3.09 | 3.64 | 4.04 | 4.51 | 4.99 |
|  | iD (mA) | 0.015 | 2.043 | 3.6003 | 4.449 | 5.1728 | 5.3674 | 5.4843 | 5.5355 | 5.56 | 5.5832 | 5.6018 |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Vdd=5[V] | |  | |  | |  | |  | |  | |  | |  | |  | |  | |  | |  | |
| **CMOS** | Vin[V] | | 0 | | 0.11 | | 0.19 | | 0.3 | | 0.41 | | 0.5 | | 0.6 | | 0.7 | | 0.8 | | 0.9 | | 1.01 | |
|  | Vout[V] | | 5.053 | | 5.053 | | 5.053 | | 5.053 | | 5.053 | | 5.053 | | 5.053 | | 5.053 | | 5.053 | | 5.053 | | 5.052 | |
|  |  | |  | |  | |  | |  | |  | |  | |  | |  | |  | |  | |  | |
| 1.1 | 1.2 | | 1.29 | | 1.4 | | 1.5 | | 1.6 | | 1.71 | | 1.8 | | 1.9 | | 2.01 | | 2.1 | | 2.2 | | 2.3 | |
| 5.049 | 5.042 | | 5.031 | | 5.007 | | 4.973 | | 4.927 | | 4.862 | | 4.788 | | 4.685 | | 4.512 | | 4.266 | | 2.814 | | 0.5498 | |
|  |  | |  | |  | |  | |  | |  | |  | |  | |  | |  | |  | |  | |
| 2.4 | 2.5 | | 2.61 | | 2.7 | | 2.8 | | 2.9 | | 3 | | 3.1 | | 3.2 | | 3.3 | | 3.4 | | 3.5 | | 3.6 | |
| 0.3374 | 0.2441 | | 0.1773 | | 0.1366 | | 0.1007 | | 0.0688 | | 0.0483 | | 0.0306 | | 0.0169 | | 0.0086 | | 0.0027 | | 0.0005 | | 0.0001 | |
|  |  | |  | |  | |  | |  | |  | |  | |  | |  | |  | |  | |  | |
| 3.7 | 3.8 | 3.9 | | 4 | | 4.1 | | 4.2 | | 4.3 | | 4.4 | | 4.5 | | 4.6 | | 4.7 | | 4.8 | | 4.9 | | 5 | |
| 0 | 0 | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | | Vdd=5[V] | |  | |  | |  | |  | |  | |  | |  | |  | |  | |  | |  | |
| **Pseudo-NMOS** | | Vin[V] | | 0 | | 0.1 | | 0.2 | | 0.3 | | 0.4 | | 0.5 | | 0.6 | | 0.7 | | 0.8 | | 0.9 | | 1 | |
|  | | Vout[V] | | 5.052 | | 5.052 | | 5.052 | | 5.052 | | 5.052 | | 5.052 | | 5.052 | | 5.052 | | 5.052 | | 5.052 | | 5.052 | |
|  | |  | |  | |  | |  | |  | |  | |  | |  | |  | |  | |  | |  | |
| 1.1 | | 1.2 | | 1.31 | | 1.4 | | 1.5 | | 1.6 | | 1.7 | | 1.8 | | 1.9 | | 2 | | 2.1 | | 2.2 | | 2.3 | |
| 5.051 | | 5.047 | | 5.039 | | 5.027 | | 5.008 | | 4.987 | | 4.956 | | 4.919 | | 4.88 | | 4.831 | | 4.781 | | 4.72 | | 4.653 | |
|  | |  | |  | |  | |  | |  | |  | |  | |  | |  | |  | |  | |  | |
| 2.4 | | 2.5 | | 2.6 | | 2.7 | | 2.8 | | 2.9 | | 3 | | 3.1 | | 3.2 | | 3.3 | | 3.4 | | 3.5 | | 3.6 | |
| 4.587 | | 4.509 | | 4.424 | | 4.333 | | 4.23 | | 4.123 | | 4.006 | | 3.881 | | 3.74 | | 3.59 | | 3.428 | | 3.249 | | 3.024 | |
| 3.7 | 3.8 | | 3.9 | | 4 | | 4.1 | | 4.2 | | 4.3 | | 4.4 | | 4.5 | | 4.6 | | 4.7 | | 4.8 | | 4.9 | | 5 | |
| 2.792 | 2.485 | | 2.147 | | 1.793 | | 1.57 | | 1.424 | | 1.324 | | 1.248 | | 1.187 | | 1.134 | | 1.089 | | 1.055 | | 1.023 | | 0.9922 | |